

THIRD SEMESTER (Common to EC/TC/EE/IT/BM/ML)

SUBJECT CODE: **06ES32**
SUBJECT: **ANALOG ELECTRONIC CIRCUITS**
(Common EC and TC)
EXAM MARKS: 100

IA MARKS: 25
EXAM HOURS: 3
HOURS / WEEK: 4
TOTAL HOURS: 52

PART – A

UNIT 1:

Diode Circuits: Diode Resistance, Diode equivalent circuits, Transition and diffusion capacitance, Reverse recovery time, Load line analysis, Rectifiers, Clippers and clampers.
(Chapter 1.6 to 1.14, 2.1 to 2.9) **06 Hours**

UNIT 2:

Transistor Biasing: Operating point, Fixed bias circuits, Emitter stabilized biased circuits, Voltage divider biased, DC bias with voltage feedback, miscellaneous bias configurations, Design operations, Transistor switching networks, PNP transistors, Bias stabilization.
(Chapter 4.1 to 4.12) **07 Hours**

UNIT 3:

Transistor at Low Frequencies: BJT transistor modeling, Hybrid equivalent model, CE Fixed bias configuration, Voltage divider bias, Emitter follower, CB configuration, Collector feedback configuration, Hybrid equivalent model. (Chapter 5.1 to 5.3, 5.5 to 5.17) **07 Hours**

UNIT 4:

Transistor Frequency Response: General frequency considerations, low frequency response, Miller effect capacitance, High frequency response, multistage frequency effects.
(Chapter 9.1 to 9.5, 9.6, 9.8, 9.9) **06 Hours**

PART – B

UNIT 5:

(a) General Amplifiers: Cascade connections, Cascode connections, Darlington connections.
(Chapter 5.19 to 5.27) **03Hours**

(b) Feedback Amplifier: Feedback concept, Feedback connections type, Practical feedback circuits. (Chapter 14.1 to 14.4) **03 Hours**

UNIT 6:

Power Amplifiers: Definitions and amplifier types, series fed class A amplifier, Transformer coupled Class A amplifiers, Class B amplifier operations, Class B amplifier circuits, Amplifier distortions. (Chapter 12.1 to 12.9) **07 Hours**

UNIT 7:

Oscillators: Oscillator operation, Phase shift Oscillator, Wienbridge Oscillator, Tuned Oscillator circuits, Crystal Oscillator. (Chapter 14.5 to 14.11) (BJT version only) **06 Hours**

UNIT 8:

FET Amplifiers: FET small signal model, Biasing of FET, Common drain common gate configurations, MOSFETs, FET amplifier networks. (Chapter 8.1 to 8.13) **07 Hours**

TEXT BOOK:

1. **Robert L. Boylestad and Louis Nashelsky**, “Electronic Devices and Circuit Theory”, PHI. 9TH Edition.

REFERENCE BOOKS:

1. **Jacob Millman & Christos C. Halkias**, ‘Integrated Electronics’, Tata -McGraw Hill, 1991 Edition

2 . **David A. Bell**, “Electronic Devices and Circuits”, PHI, 4th Edition, 2004

Question Paper Pattern: Student should answer FIVE full questions out of 8 questions to be set each carrying 20 marks, **selecting at least TWO questions from each part.**

SUBJECT CODE: **06ES 33**
SUBJECT: LOGIC DESIGN
(Common EC/TC/EE/IT/BM/ML)
EXAM MARKS: 100

IA MARKS: 25
EXAM HOURS: 3
HOURS / WEEK: 4
TOTAL HOURS: 52

Part –A

Unit 1:

Principles of combinational logic-1: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3, 4 and 5 variables, Incompletely specified functions (Don't Care terms), Simplifying Max term equations. [(Text book 1) 3.1, 3.2, 3.3, 3.4] **7 Hours**

Unit 2:

Principles of combinational Logic-2: Quine-McCluskey minimization technique- Quine-McCluskey using don't care terms, Reduced Prime m Implicant Tables, Map entered variables [(Text book 1) 3.5, 3.6] **7 Hours**

Unit 3:

Analysis and design of combinational logic - I: General approach, Decoders-BCD decoders, Encoders. [(Text book 1) 4.1, 4.3, 4.4] **6 Hours**

Unit 4:

Analysis and design of combinational logic - II: Digital multiplexers- Using multiplexers as Boolean function generators. Adders and subtractors - Cascading full adders, Look ahead carry, Binary comparators. [(Text book 1) 4.5, 4.6 - 4.6.1, 4.6.2, 4.7] **6 Hours**

Part –B

Unit 5:

Sequential Circuits – 1: Basic Bistable Element, Latches, SR Latch, Application of SR Latch, A Switch Debouncer, The **R S** Latch, The gated SR Latch, The gated D Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The Master-Slave SR Flip-Flops, The Master-Slave JK Flip-Flop, Edge Triggered Flip-Flop: The Positive Edge-Triggered D Flip-Flop, Negative-Edge Triggered D Flip-Flop. [(Text book 2) 6.1, 6.2, 6.4, 6.5] **7 Hours**

Unit 6:

Sequential Circuits – 2: Characteristic Equations, Registers, Counters - Binary Ripple Counters, Synchronous Binary counters, Counters based on Shift Registers, Design of a Synchronous counters, Design of a Synchronous Mod-6 Counter using clocked JK Flip-Flops Design of a Synchronous Mod-6 Counter using clocked D, T, or SR Flip-Flops [(Text book 2) 6.6, 6.7, 6.8, 6.9 – 6.9.1 and 6.9.2] **7 Hours**

Unit 7:

Sequential Design - I: Introduction, Mealy and Moore Models, State Machine Notation, Synchronous Sequential Circuit Analysis, [(Text book 1) 6.1, 6.2, 6.3] **6 Hours**

Unit 8:

Sequential Design - II: Construction of state Diagrams, Counter Design [(Text book 1) 6.4, 6.5] **6 Hours**

Text books:

1. John M Yarbrough, "Digital Logic Applications and Design", Thomson Learning, 2001.
2. Donald D Givone, "Digital Principles and Design", Tata McGraw Hill Edition, 2002.

Reference Books:

1. Charles H Roth, Jr; "Fundamentals of logic design", Thomson Learning, 2004.
2. Mono and Kim, "Logic and computer design Fundamentals", Pearson, Second edition, 2001.

Coverage of the Text Books:

Unit 1: (Text book 1) 3.1, 3.2, 3.3, 3.4

Unit 2: (Text book 1) 3.5, 3.6

Unit 3: (Text book 1) 4.1, 4.3, 4.4

Unit 4: [(Text book 1) 4.5, 4.6 - 4.6.1, 4.6.2, 4.7

Unit 5: (Text book 2) 6.1, 6.2, 6.4, 6.5

Unit 6: (Text book 2) 6.6, 6.7, 6.8, 6.9 – 6.9.1 and 6.9.2

Unit 7: (Text book 1) 6.1, 6.2, 6.3

Unit 8: (Text book 1) 6.4, 6.5

SUBJECT CODE: **06ES34**
SUBJECT: **NETWORK ANALYSIS**
(Common EC/TC/EE/IT/BM/ML)
HOURS / WEEK: 4

IA MARKS: 25
EXAM HOURS: 3
EXAM MARKS: 100
TOTAL HOURS: 52

PART – A

UNIT 1:

Basic Concepts: Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis With linearly dependent and independent sources for DC and AC networks, Concepts of super node and super mesh **07 Hours**

UNIT 2:

Network Topology: Graph of a network, Concept of tree and co-tree, incidence matrix, tie -set, tie-set and cut-set schedules, Formulation of equilibrium equations in matrix form, Solution of resistive networks, Principle of duality. **07 Hours**

UNIT 3:

Network Theorems – I: Superposition, Reciprocity and Millman's theorems

06 Hours

UNIT 4:

Network Theorems - II: Thevenin's and Norton's theorems; Maximum Power transfer theorem

06 Hours

PART – B

UNIT 5: Resonant Circuits: Series and parallel resonance, frequency response of series and Parallel circuits, Q –factor, Bandwidth. **06Hours**

UNIT 6:

Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations. **07 Hours**

UNIT 7:

Laplace Transformation & Applications: Solution of networks, step, ramp and impulse responses, waveform Synthesis **07 Hours**

UNIT 8:

Two port network parameters: Definition of z, y, h and transmission parameters, modeling with these parameters, relationship between parameters Sets **06 Hours**

TEXT BOOKS:

1. **M. E. Van Valkenburg**, "Network Analysis", PHI / Pearson Education, 3rd Edition. Reprint 2002

2. **Roy Choudhury**, "Networks and systems", 2nd edition, 2006 re-print, New Age International Publications

REFERENCE BOOKS :

1. **Hayt, Kemmerly and Durbin**, "Engineering Circuit Analysis", TMH 6th Edition, 2002

2. **Franklin F. Kuo**, "Network analysis and Synthesis", Wiley International Edition,

3. **David K. Cheng**, "Analysis of Linear Systems", Narosa Publishing House, 11th reprint, 2002

4. **A. Bruce Carlson**, "Circuits", Thomson Learning, 2000. Reprint 2002 **Question Paper Pattern:** Student should answer FIVE full questions out of 8 questions to be set each carrying 20 marks, selecting at least TWO questions from each part.

Coverage in the Texts:

Unit 1: Text 2: 1.6, 2.3, 2.4 (Also refer **R1**:2.4, 4.1 to 4.6; 5.3, 5.6; 10.9

This book gives concepts of super node and super mesh)

Unit 2: Text 2: 3.1 to 3.11

Unit 3 and Unit 4: Text 2 – 7.1 to 7.7

Unit 5: Text 2 – 8.1 to 8.3

Unit 6: Text 1 – Chapter 5;

Unit 7: Text 1 – 7.4 to 7.7; 8.1 to 8.5

Unit 8: Text 1 – 11.1 to 11.6

SUBJECT CODE: 06 IT35
SUBJECT: ELECTRONIC INSTRUMENTATION
(Common to EC/TC/IT/BM/ML)
HOURS / WEEK: 4
PART – A

IA MARKS: 25
EXAM HOURS: 3
EXAM MARKS: 100
TOTAL HOURS: 52

UNIT – 1: Introduction

(a) Measurement Errors: Gross errors and systematic errors, Absolute and relative errors, Accuracy, Precision, Resolution and Significant figures. (Text 2: 2.1 to 2.3)

(b) Voltmeters and Multimeters Introduction, Multirange voltmeter, Extending voltmeter ranges, Loading, AC voltmeter using Rectifiers – Half wave and full wave, Peak responding and True RMS voltmeters. (Text 1: 4.1, 4.4 to 4.6, 4.12 to 4.14, 4.17, 4.18) **07 Hours**

UNIT – 2: Digital Instruments Digital Voltmeters – Introduction, DVM's based on V – T, V – F and Successive approximation principles, Resolution and sensitivity, General specifications, Digital Multi-meters, Digital frequency meters, Digital measurement of time (Text 1: 5.1 to 5.6; 5.9 and 5.10; 6.1 to 6.4) **07 Hours**

UNIT – 3: Oscilloscopes Introduction, Basic principles, CRT features, Block diagram and working of each block, Typical CRT connections, Dual beam and dual trace CROs, Electronic switch (Text 1: 7.1 to 7.9, 7.12, 7.14 to 7.16) **06 Hours**

UNIT – 4: Special Oscilloscopes Delayed time -base oscilloscopes, Analog storage, Sampling and Digital storage oscilloscopes (Text 2: 10.1 to 10.4) **06 Hours**

PART – B

UNIT – 5: Signal Generators Introduction, Fixed and variable AF oscillator, Standard signal generator, Laboratory type signal generator, AF sine and Square wave generator, Function generator, Square and Pulse generator, Sweep frequency generator, Frequency synthesizer (Text 1: 8.1 to 8.9 and Text 2: 11.5, 11.6) **06 Hours**

UNIT – 6: Measurement of resistance, inductance and capacitance Whetstone's bridge, Kelvin Bridge; AC bridges, Capacitance Comparison Bridge, Maxwell's bridge, Wein's bridge, Wagner's earth connection (Text 1: 11.1 to 11.3, 11.8, 11.9, 11.11, 11.14 and 11.15) **07 Hours**

UNIT – 7: Transducers – I Introduction, Electrical transducers, Selecting a transducer, Resistive transducer, Resistive position transducer, Strain gauges, Resistance thermometer, Thermistor, Inductive transducer, Differential output transducers and LVDT, (Text 1: 13.1 to 13.11) **07 Hours**

UNIT – 8: Miscellaneous Topics (a) Transducers - II –Piezoelectric transducer, Photoelectric transducer, Photovoltaic transducer, Semiconductor photo devices, Temperature transducers- RTD, Thermocouple (Text 1: 13.15 to 13.20)

(b) Display devices: Digital display system, classification of display, Display devices, LEDs, LCD displays (Text 1: 2.7 to 2.11)

(c) Bolometer and RF power measurement using Bolometer (Text 1: 20.1 to 20.9)

(d) Introduction to Signal conditioning (Text 1: 14.1) **06 Hours**

TEXT BOOKS:

1. H. S. Kalsi, "Electronic Instrumentation", TMH, 2004
2. David A Bell, "Electronic Instrumentation and Measurements" PHI / Pearson Education, 2006.

REFERENCE BOOKS:

1. John P. Beately, "Principles of measurement systems", 3rd Edition, Pearson Education, 2000
2. Cooper D & A D Helfrick, "Modern electronic instrumentation and measuring techniques", PHI, 1998.
3. J. B. Gupta, "Electronic and Electrical measurements and Instrumentation", S. K. Kataria & Sons, Delhi
4. A K Sawhney, Electronics & electrical measurements, Dhanpat Rai & sons, 9th edition.

Question Paper Pattern: Student should answer FIVE full questions out of 8 questions to be set each carrying 20 marks, **selecting at least TWO questions from each part Coverage in the**

Texts:

UNIT – 1: (a) Text 2: 2.1 to 2.3; (b) Text 1: 4.1, 4.4 to 4.6, 4.12 to 4.14, 4.17, 4.18

UNIT – 2: Text 1: 5.1 to 5.6; 5.9 and 5.10; 6.1 to 6.4

UNIT – 3: Text 1: 7.1 to 7.9, 7.12, 7.14 to 7.16

UNIT – 4: Text 2: 10.1 to 10.5

UNIT – 5: Text 1: 8.1 to 8.9 and Text 2: 11.5, 11.6

UNIT – 6: Text 1: 11.1 to 11.3, 11.8, 11.9, 11.11, 11.14 and 11.15

UNIT – 7: Text 1: 13.1 to 13.11

UNIT – 8: (a) Text 1: 13.15 to 13.20.2 (b) Text 1: 2.7 to 2.12 (c) Text 1: 20.1 to 20.9 (d) Text 1: 14.1

SUBJECT CODE: **06ES 36 / 44**
SUBJECT: **FIELD THEORY**
(Common to EC/TC/ML/EE)
HOURS / WEEK: 4

IA MARKS: 25
EXAM HOURS: 3
EXAM MARKS: 100
TOTAL HOURS: 52

PART – A

UNIT 1:

a. Coulomb's Law and electric field intensity: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge (Chapter 2 – 2.1, 2.2, 2.3 2.4) **03 Hours**

b. Electric flux density, Gauss' law and divergence: Electric flux density, Gauss' law, Divergence, Maxwell's First equation(Electrostatics), vector operator $\vec{\nabla}$ and divergence theorem(Chapter 3 – 3.1, 3.2, 3.5, 3.6, 3.7) **04 Hours**

UNIT 2:

a. Energy and potential : Energy expended in moving a point charge in an electric field, The line integral, Definition of potential difference and Potential, The potential field of a point charge and system of charges, Potential gradient , Energy density in an electrostatic field (Chapter 4 – 4.1, 4.2, 4.3, 4.4, 4.5 4.6, 4.8) **04 Hours**

b. Conductors, dielectrics and capacitance: Current and current density, Continuity of current, metallic conductors, Conductor properties and boundary conditions, boundary conditions for perfect Dielectrics, capacitance and examp les. (Chapter 5 - 5.1, 5.2, 5.3, 5.4; Chapter 6 – 6.2, 6.3, 6.4) **03 Hours**

UNIT 3:

Poisson's and Laplace's equations: Derivations of Poisson's and Laplace's Equations, Uniqueness theorem, Examples of the solutions of Laplace's and Poisson's equations (Chapter 7 – 7.1, 7.2, 7.3, 7.4) **06 Hours**

UNIT 4:

The steady magnetic field: Biot-Savart law, Ampere's circuital law, Curl, Stokes' theorem, magnetic flux and flux density, scalar and Vector magnetic potentials (Chapter 8 – 8.1, 8.2, 8.3, 8.4, 8.5, 8.6) **06 Hours**

PART – B

UNIT 5:

a. Magnetic forces: Force on a moving charge and differential current element, Force between differential current elements, Force and torque on a closed circuit. (Chapter 9 – 9.1, 9.2, 9.3, 9.4) **03 Hours**

b. Magnetic materials and inductance: Magnetization and permeability, Magnetic boundary conditions, Magnetic circuit, Potential energy and forces on magnetic materials, Inductance and Mutual Inductance.(Chapter 9 – 9.6, 9.7, 9.8, 9.9, 9.10) **04 Hours**

UNIT 6:

Time varying fields and Maxwell's equations: Faraday's law, displacement current, Maxwell's equation in point and Integral form, retarded potentials(Chapter 10) **06 Hours**

UNIT 7:

Uniform plane wave: Wave propagation in free space and dielectrics, Poynting's theorem and wave power, propagation in good conductors – (skin effect). (Chapter 12 – 12.1 to 12.4) **07 Hr**

UNIT 8:

Plane waves at boundaries and in dispersive media: Reflection of uniform plane waves at normal incidence, SWR, Plane wave propagation in general directions. (Chapter 13 – 13.1, 13.2, 13.4) **06 Hours**

TEXT BOOK:

William H Hayt Jr. and John A Buck, "Engineering Electromagnetics", Tata McGraw-Hill, 7th edition, 2006

REFERENCE BOOKS :

1. John Krauss and Daniel A Fleisch, "Electromagnetics with Applications", McGraw-Hill, 5th edition, 1999
2. Edward C. Jordan and Keith G Balmain, "Electromagnetic Waves And Radiating Systems," Prentice – Hall of India / Pearson Education, 2nd edition, 1968.Reprint 2002
3. David K Cheng, "Field and Wave Electromagnetics" Pearson Education Asia, 2nd edition, - 1989, Indian Reprint – 2001.

Question Paper Pattern: Student should answer FIVE full questions out of 8 questions to be set each carrying 20 marks, **selecting at least TWO questions from each part Coverage in the**

Text book:

UNIT 1: (a) Chapter 2 (b) Chapter 3

UNIT 2: (a) Chapter 4 except section 4.7

(b) Chapter 5 (except sections 5.5 and 5.6); 6.2, 6.3, 6.4

UNIT 3: Chapter 7 except sections 7.5 and 7.6

UNIT 4: Chapter 8 except section 8.7

UNIT 5: Chapter 9 except Section 9.5

UNIT 6: Chapter 10

UNIT 7: Chapter 12

UNIT 8: Chapter 13 – 13.1, 13.2, 13.4, 13.7

SUBJECT CODE: **06ESL 37**
SUBJECT: **ANALOG ELECTRONICS LAB**
(Common to EC/TC/EE/IT/BM/ML)
HOURS / WEEK: 3

IA MARKS: 25
EXAM HOURS: 3
EXAM MARKS: 50

1. Wiring of RC coupled Single stage FET & BJT amplifier and determination of the gain-frequency response, input and output impedances.
2. Wiring of BJT Darlington Emitter follower with and without bootstrapping and determination of the gain, input and output impedances (Single circuit) (One Experiment)
3. Wiring of a two stage BJT Voltage series feed back amplifier and determination of the gain, Frequency response, input and output impedances with and without feedback (One Experiment)
4. Wiring and Testing for the performance of BJT-RC Phase shift Oscillator for $f_0 = 10$ KHz
5. Testing for the performance of BJT – Hartley & Colpitts Oscillators for RF range $f_0=100$ KHz.
6. Testing for the performance of BJT -Crystal Oscillator for $f_0 > 100$ KHz
- 7 Testing of Diode clipping (Single/Double ended) circuits for peak clipping, peak detection
8. Testing of Clamping circuits: positive clamping /negative clamping.
9. Testing of a transformer less Class – B push pull power amplifier and determination of its conversion efficiency.
10. Testing of Half wave, Full wave and Bridge Rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency
11. Verification of Thevinin's Theorem and Maximum Power Transfer theorem for DC Circuits.
12. Characteristics of Series and Parallel resonant circuits.

SUBJECT CODE: **06ESL 38**
SUBJECT: LOGIC DESIGN LAB
(Common to EC/TC/EE/IT/BM/ML)
HOURS / WEEK: 3

IA MARKS: 25
EXAM HOURS: 3
EXAM MARKS: 50

1. Simplification, realization of Boolean expressions using logic gates/Universal gates.
2. Realization of Half/Full adder and Half/Full Subtractors using logic gates.
3. (i) Realization of parallel adder/Subtractors using 7483 chip
(ii) BCD to Excess-3 code conversion and vice versa.
4. Realization of Binary to Gray code conversion and vice versa
5. MUX/DEMUX – use of 74153, 74139 for arithmetic circuits and code converter.
6. Realization of One/Two bit comparator and study of 7485 magnitude comparator.
7. Use of a) Decoder chip to drive LED display and b) Priority encoder.
8. Truth table verification of Flip-Flops: (i) JK Master slave (ii) T type and (iii) D type.
9. Realization of 3 bit counters as a sequential circuit and MOD – N counter design (7476, 7490, 74192, 74193).
10. Shift left; Shift right, SIPO, SISO, PISO, PIPO operations using 74S95.
11. Wiring and testing Ring counter/Johnson counter.
12. Wiring and testing of Sequence generator.

FOURTH SEMESTER

SUBJECT CODE: 06ES42
SUBJECT: MICROCONTROLLERS
(Common to, EE, EC, IT, TC, BM and ML)
HOURS / WEEK: 4

IA MARKS: 25
EXAM HOURS: 3
EXAM MARKS: 100
TOTAL HOURS: 52

PART – A

UNIT 1:

Microprocessors and microcontroller. Introduction, Microprocessors and Microcontrollers, A Microprocessors survey. RISC & CISC CPU Architectures, Harvard & Von-Neumann CPU architecture.

The 8051 Architecture: Introduction, 8051 Microcontroller Hardware, Input / Output Pins, Ports and Circuits External Memory, Counter and Timers, Serial Data Input / Output, Interrupts.

07 Hrs

UNIT 2:

Addressing Modes and Operations: Introduction, Addressing modes, External data Moves, Code Memory, Read Only Data Moves / Indexed Addressing mode, PUSH and POP Opcodes, Data exchanges, Example Programs; Byte level logical Operations, Bit level Logical Operations, Rotate and Swap Operations, Example Programs. Arithmetic Operations: Flags, Incrementing and Decrementing, Addition, Subtraction, Multiplication and Division, Decimal Arithmetic, Example Programs.

07 Hrs.

UNIT 3:

Jump and Call Instructions: The JUMP and CALL Program range, Jumps, calls and Subroutines, Interrupts and Returns, More Detail on Interrupts, Example Problems

06 Hrs.

UNIT 4:

8051 programming in C: Data types and time delays in 8051C, I/O programming, logic operations, data conversion programs, accessing code ROM space, data serialization.

06 Hrs

PART – B

UNIT 5:Timer / Counter Programming in 8051: Programming 8051 Timers, Counter Programming, programming timers 0 and 1 in 8051 C

06 Hrs

UNIT 6:

8051 Serial Communication: Basics of Serial Communication, 8051 connections to RS-232, 8051 Serial communication Programming, Programming the second serial port, Serial port programming in C.

07 Hrs

UNIT 7:

Interrupts Programming: 8051 Interrupts, Programming Timer Interrupts, Programming External Hardware Interrupts, Programming the Serial Communication Interrupts, Interrupt Priority in the 8051/52, interrupt programming in C

06 Hrs

UNIT 8:

8051 Interfacing and Applications: Interfacing 8051 to LCD, Keyboard, parallel and serial ADC, DAC, Stepper motor interfacing, DC motor interfacing and PWM

07 Hrs

Text Books:

1. **Kenneth J. Ayala;** “The 8051 Microcontroller Architecture, Programming & Applications” 2e, Penram International, 1996 / Thomson Learning 2005

2. **Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay;** “The 8051 Microcontroller and Embedded Systems – using assembly and C”- PHI, 2006 / Pearson, 2006

Reference Books:

1. **Predko ;** “Programming and Customizing the 8051 Microcontroller” –, TMH

2. **Raj Kamal,** “Microcontrollers: Architecture, Programming, Interfacing and System Design”, Pearson Education, 2005

3. **Ajay V.Deshmukh;** “Microcontrollers- Theory and Applications”, TMH, 2005

4. **Dr.Ramani Kalpathi and Ganesh Raja;** “Microcontroller and its

Applications”, Sanguine Technical publishers, Bangalore-2005 **Question Paper Pattern:** Student should answer FIVE full questions out of 8 questions to be set each carrying 20 marks, selecting at least TWO questions from each part

Coverage in the Text books:

UNIT 1: Text 1 – Chapter 1(excluding 1.2 and 1.4) and chapter 3, R1 - Chapter 1

UNIT 2: Text 1-chapters 5, 6 & 7

UNIT 3: Text 1 - chapter 8

UNIT 4: Text 2 – chapter 7

UNIT 5: Text 2 – chapter 9

UNIT 6: Text 2 – chapter 10

UNIT 7: Text 2 – chapter 11

UNIT 8: Text 2 – chapter 12, chapter 13(13.1&13.2), chapter 17 (except 17.1)

SUBJECT CODE: **06ES43**
SUBJECT: **CONTROL SYSTEMS**
(Common to EC/TC/EE/IT/BM/ML)
HOURS / WEEK: 4

IA MARKS: 25
EXAM HOURS: 3
EXAM MARKS: 100
TOTAL HOURS: 52

PART – A

UNIT 1:

Modeling of Systems: The control system, Mathematical models of physical systems – Introduction, Differential equations of physical systems – Mechanical systems, Friction, Translational systems (Mechanical accelerometer, Levered systems excluded), Rotational systems, Gear trains, Electrical systems, Analogous systems **06 Hours**

UNIT 2:

Block diagrams and signal flow graphs: Transfer functions, Block diagram algebra, Signal Flow graphs (State variable formulation excluded), **07 Hours**

UNIT 3:

Time Response of feed back control systems: Standard test signals, Unit step response of First and second order systems, Time response specifications, Time response specifications of second order systems, steady – state errors and error constants. **07 Hours**

UNIT 4:

Stability analysis: Concepts of stability, Necessary conditions for Stability, Routh- stability criterion, Relative stability analysis; More on the Routh stability criterion **06 Hours**

PART – B

UNIT 5:

Root–Locus Techniques: Introduction, The root locus concepts, Construction of root loci. **06 Hours**

UNIT 6:

Stability in the frequency domain: Mathematical preliminaries, Nyquist Stability criterion, (Inverse polar plots excluded), Assessment of relative stability using Nyquist criterion, (Systems with transportation lag excluded). **07 Hours**

UNIT 7:

Frequency domain analysis: Introduction, Correlation between time and frequency response, Bode plots, All pass and minimum phase systems, Experimental determination of transfer functions, Assessment of relative stability using Bode Plots. **07 Hours**

UNIT 8:

Introduction to State variable analysis: Concepts of state, state variable and state models for electrical systems, Solution of state equations. **06 Hours**

TEXT BOOK :

1. **J. Nagarath and M.Gopal**, “Control Systems Engineering”, New Age International (P) Limited, Publishers, Fourth edition – 2005

REFERENCE BOOKS:

1. K. Ogata, “Modern Control Engineering “, Pearson Education Asia/ PHI, 4th Edition, 2002.
2. P. S. Satyanarayana; “Concepts of Control Systems”, Dynaram publishers, Bangalore, 2001
3. M. Gopal, “Control Systems – Principles and Design”, TMH, 1999
4. J. J. D’Azzo and C. H. Houpis; “Feedback control system analysis and synthesis”, McGraw Hill, International student Edition.

Question Paper Pattern: Student should answer FIVE full questions out of 8 questions to be set each carrying 20 marks, **selecting at least TWO questions from each part**

COVERAGE IN THE TEXT BOOK:

UNIT 1: 1.1, 2.1, 2.2, 2.7

UNIT 2: 2.4, 2.5, 2.6, 2.7

UNIT 3: 5.1, 5.2, 5.3, 5.4, 5.5

UNIT 4: 6.1, 6.2, 6.4, 6.5, 6.6

UNIT 5: 7.1, 7.2, 7.3

UNIT 6: 9.1, 9.2, 9.3, 9.4,

UNIT 7: 8.1, 8.2, 8.4, 8.5, 8.6

UNIT 8: 12.1, 12.2, 12.3, 12.6

SUBJECT CODE: **06EC 44**
SUBJECT: **SIGNALS & SYSTEMS**
(Common to EC/TC/IT/BM/ML)
HOURS / WEEK: 4

IA MARKS: 25
EXAM HOURS: 3
EXAM MARKS: 100
TOTAL HOURS: 52

PART – A

UNIT 1:

Introduction: Definitions of a signal and a system, classification of signals, basic Operations on signals, elementary signals, Systems viewed as Interconnections of operations, properties of systems. **07 Hours**

UNIT 2:

Time-domain representations for LTI systems – 1: Convolution, impulse response representation, Convolution Sum and Convolution Integral. **06 Hours**

UNIT 3:

Time-domain representations for LTI systems – 2: properties of impulse response representation, Differential and difference equation Representations, Block diagram representations. **07 Hours**

UNIT 4:

Fourier representation for signals – 1: Introduction, Discrete time and continuous time Fourier series (derivation of series excluded) and their properties. **06 Hours**

PART – B

UNIT 5:

Fourier representation for signals – 2: Discrete and continuous Fourier transforms (derivations of transforms are excluded) and their properties. **06 Hours**

UNIT 6:

Applications of Fourier representations: Introduction, Frequency response of LTI systems, Fourier transform representation of periodic signals, Fourier transform representation of discrete time signals **07 Hours**

UNIT 7:

Z-Transforms – 1: Introduction, Z – transform, properties of ROC, properties of Z – transforms, inversion of Z – transforms. **07 Hours**

UNIT 8:

Z-transforms – 2: Transform analysis of LTI Systems, unilateral ZTransform and its application to solve difference equations. **06 Hours**

TEXT BOOK

Simon Haykin and Barry Van Veen “Signals and Systems”, John Wiley & Sons, 2001.Reprint 2002

REFERENCE BOOKS :

1. **Alan V Oppenheim, Alan S, Willsky and A Hamid Nawab**, “Signals and Systems” Pearson Education Asia / PHI, 2nd edition, 1997. Indian Reprint 2002
2. **H. P Hsu, R. Ranjan**, “Signals and Systems”, Scham’s outlines, TMH, 2006
3. **B. P. Lathi**, “Linear Systems and Signals”, Oxford University Press, 2005
4. **Ganesh Rao and Satish Tunga**, “Signals and Systems”, Sanguine Technical Publishers, 2004

Question Paper Pattern: Student should answer FIVE full questions out of 8 questions to be set each carrying 20 marks, **selecting at least TWO questions from each part**

Coverage in the Text:

UNIT 1: 1.1, 1.2, 1.4 to 1.8

UNIT 2: 2.1, 2.2

UNIT 3: 2.3, 2.4, 2.5

UNIT 4: 3.1, 3.2, 3.3, 3.6

UNIT 5: 3.4, 3.5, 3.6

UNIT 6: 4.1, 4.2, 4.3, 4.5, 4.6.

UNIT 7: 7.1, 7.2, 7.3, 7.4, 7.5

UNIT 8: 7.6 (Excluding ‘relating the transfer function and the State-Variable description, determining the frequency response from poles and zeros) and 7.8

SUBJECT CODE: 06EC45
(Common EC/TC/IT/BM/ML)
HOURS/WEEK: 4
EXAM HOURS: 3

SUBJECT: FUNDAMENTALS OF HDL
IA MARKS: 25
TOTAL HOURS: 52
EXAM MARKS: 100

PART-A

UNIT 1:

Introduction: Why HDL? , A Brief History of HDL, Structure of HDL Module, Operators, Data types, Types of Descriptions, simulation and synthesis, Brief comparison of VHDL and Verilog
6 HRS

UNIT 2:

Data –Flow Descriptions: Highlights of Data-Flow Descriptions, Structure of Data-Flow Description, Data Type – Vectors
6 HRS

UNIT 3:

Behavioral Descriptions: Behavioral Description highlights, structure of HDL behavioral Description, The VHDL variable –Assignment Statement, sequential statements.
7 HRS

UNIT 4:

Structural Descriptions: Highlights of structural Description, Organization of the structural Descriptions, Binding, state Machines, Generate, Generic and Parameter statements.
7 HRS

PART-B

UNIT 5: Procedures, Tasks, and Functions: Highlights of Procedures, tasks, and Functions, Procedures and tasks, Functions. **Advanced HDL Descriptions:** File Processing, Examples of File Processing
7 HRS

UNIT 6:

Mixed –Type Descriptions: Why Mixed-Type Description? VHDL User-Defined Types, VHDL Packages, Mixed-Type Description examples
6HRS

UNIT 7:

Mixed –Language Descriptions: Highlights of Mixed-Language Description, How to invoke One language from the Other, Mixed-language Description Examples, Limitations of Mixed-Language Description
7 HRS

UNIT 8:

Synthesis Basics: Highlights of Synthesis, Synthesis information from Entity and Module, Mapping Process and Always in the Hardware Domain.
6HRS

Text Books:

1. HDL Programming (VHDL and Verilog)- Nazeih M.Botros- Dreamtech Press (Available through John Wiley – India and Thomson Learning) 2006 Edition

Reference Books:

1. Verilog HDL –Samir Palnitkar-Pearson Education
2. VHDL -Douglas perry-Tata McGraw-Hill
3. A Verilog HDL Primer- J.Bhaskar – BS Publications
4. Circuit Design with VHDL-Volnei A.Pedroni-PHI

SUBJECT CODE: **06EC 46**
SUBJECT: **LINEAR IC's AND APPLICATIONS**
(Common to EC/TC/IT/ML/BM)
HOURS / WEEK: 4

IA MARKS: 25
EXAM HOURS: 3
EXAM MARKS: 100
TOTAL HOURS: 52

PART - A

UNIT 1:

Operational Amplifier Fundamentals: Basic Op -Amp circuit, Op-Amp parameters – Input and output voltage, CMRR and PSRR, offset voltages and currents, Input and output impedances, Slew rate and Frequency limitations; Op-Amps as DC Amplifiers- Biasing Op-Amps, Direct coupled –Voltage Followers, Non-inverting Amplifiers, Inverting amplifiers, Summing amplifiers, Difference amplifier. (Text 1: Chapter 1 – 1.2, Chapter 2 – 2.1, 2.2, 2.3, 2.4, 2.5, and Chapter 3 – 3.1, 3.2, 3.3, 3.4, 3.5, 3.6) **7 Hours**

UNIT 2:

Op-Amps as AC Amplifiers: Capacitor coupled Voltage Follower, High input impedance - Capacitor coupled Voltage Follower, Capacitor coupled Non-inverting Amplifiers, High input impedance - Capacitor coupled No inverting Amplifiers, Capacitor coupled Inverting amplifiers, setting the upper cut-off frequency, Capacitor coupled Difference amplifier, Use of a single polarity power supply. (Text 1: Chapter 4) **6 Hours**

UNIT 3:

Op-Amps frequency response and compensation: Circuit stability, Frequency and phase response, Frequency compensating methods, Band width, Slew rate effects, Zin Mod compensation, and circuit stability precautions. (Text 1: Chapter 5 – 5.1, 5.2, 5.3, 5.5, 5.6, 5.9, 5.10) **6 Hours**

UNIT 4:

OP-AMP Applications: Voltage sources, current sources and current sinks, Current amplifiers, instrumentation amplifier, precision rectifiers, Limiting circuits, (Text 1: Chapter 6 – 6.1, 6.2, 6.4, 6.8, and Chapter 7 – 7.1, 7.2, 7.3) **7 Hours**

PART – B

UNIT 5:

More applications: Clamping circuits, Peak detectors, sample and hold circuits, V to I and I to V converters, Log and antilog amplifiers, Multiplier and divider, Triangular / rectangular wave generators, Wave form generator design, phase shift oscillator, Wein bridge oscillator. (Text 1: Chapter 7 – 7.4, 7.5, 7.6; Chapters 10 -10.1, 10.2, 10.3, 10.5; Text 2: Sections 4.5, 4.8 and 4.9) **6 Hours**

UNIT 6:

Non-linear circuit applications: crossing detectors, inverting Schmitt trigger circuits, Monostable & Astable multivibrator, Active Filters –First and second order Low pass & High pass filters. (Text 1: Chapter 9 – 9.2, 9.3, 9.5, 9.6; Chapter 11 – 11.2, 11.3, 11.4, 11.5) **7 Hours**

UNIT 7:

Voltage Regulators: Introduction, Series Op-Amp regulator, IC Voltage regulators, 723 general purpose regulator, Switching regulator. (Text 2: Chapter 6) **6 Hours**

UNIT 8:

Other Linear IC applications: 555 timer - Basic timer circuit, 555 timer used as astable and monostable multivibrator, Schmitt trigger; PLL-operating principles, Phase detector / comparator, VCO; D/A and A/ D converters – Basic DAC Techniques, AD converters(Text 2: Chapter 8 – 8.1, 8.2, 8.3, 8.4, 8.5; Chapter 9 – 9.1, 9.2, 9.3, 9.4; Chapter 10 – 10. 1, 10.2, 10.3 ; Except 8.3.1, 8.4.1, 10.2.5, 10.4) **7 Hours**

TEXT BOOKS:

1. **David A. Bell**, “Operational Amplifiers and Linear IC’s”, 2nd edition, PHI/Pearson, 2004
2. **D. Roy Choudhury and Shail B. Jain**, “Linear Integrated Circuits”, 2nd edition, Reprint 2006, New Age International

REFERENCE BOOKS:

1. **Ramakant A. Gayakwad**, “Op - Amps and Linear Integrated Circuits”, 4th edition, PHI,
2. **Robert. F. Coughlin & Fred.F. Driscoll**, “Operational Amplifiers and Linear Integrated Circuits”, PHI/Pearson, 2006
3. **James M. Fiore**, “Op - Amps and Linear Integrated Circuits”, Thomson Learning, 2001

4. **Sergio Franco**, “Design with Operational Amplifiers and Analog Integrated Circuits”, TMH, 3e, 2005

Question Paper Pattern: Student should answer FIVE full questions out of 8 questions to be set each carrying 20 marks, **selecting at least TWO questions from each part**

Coverage in the Text books:

UNIT 1: (Text 1: Chapter 1 – 1.2, Chapter 2 – 2.1, 2.2, 2.3, 2.4, 2.5, and Chapter 3 – 3.1, 3.2, 3.3, 3.4, 3.5, 3.6)

UNIT 2: Text 1: Chapter 4

UNIT 3: Text 1: (Text 1: Chapter 5 – 5.1, 5.2, 5.3, 5.5, 5.6, 5.9, 5.10)

UNIT 4: (Text 1: Chapter 6 – 6.1, 6.2, 6.4, 6.8, and Chapter 7 – 7.1, 7.2, 7.3)

UNIT 5: (Text 1: Chapter 7 – 7.4, 7.5, 7.6; Chapters 10 -10.1, 10.2, 10.3, 10.5; Text 2: Sections 4.5, 4.8 and 4.9)

UNIT 6: Text 1: Chapter 9 – 9.2, 9.3, 9.5, 9.6; Chapter 11 – 11.2, 11.3, 11.4, 11.5

UNIT 7: Text 2: Chapter 6

UNIT 8: Text 2: Chapter 8 – 8.1, 8.2, 8.3, 8.4, 8.5; Chapter 9 – 9.1, 9.2, 9.3, 9.4; Chapter 10 – 10. 1, 10.2, 10.3; Except 8.3.1, 8.4.1, 10.2.5, 10.4

SUBJECT CODE: **06ESL47**
SUBJECT: **MICROCONTROLLERS LAB**
(Common to, EE, EC, IT, TC, BM and ML)
HOURS / WEEK: 3

IA MARKS: 25
EXAM HOURS: 3
EXAM MARKS: 50
TOTAL HOURS: 42

I. PROGRAMMING

1. Data Transfer - Block move, Exchange, Sorting, Finding largest element in an array
2. Arithmetic Instructions - Addition/subtraction, multiplication and division, square, Cube – (16 bits Arithmetic operations – bit addressable)
3. Counters
4. Boolean & Logical Instructions (Bit manipulations)
5. Conditional CALL & RETURN
6. Code conversion: BCD – ASCII; ASCII – Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX
7. Programs to generate delay, Programs using serial port and on-Chip timer / counter

II. INTERFACING:

Write C programs to interface 8051 chip to Interfacing modules to develop single chip solutions

8. Simple Calculator using 6 digit seven segment display and Hex Keyboard interface to 8051
9. Alphanumeric LCD panel and Hex keypad input interface to 8051
10. External ADC and Temperature control interface to 8051
11. Generate different waveforms Sine, Square, Triangular, Ramp etc. using DAC interface to 8051; change the frequency and amplitude
12. Stepper and DC motor control interface to 8051
13. Elevator interface to 8051

Subject: HDL LAB (Common to EC/TC/IT/BM/ML)

Sub Code: 06ECL48

Hrs / Week : 03

Total Hrs. : 42

Marks : 25

Exam Hours : 03

Exam Marks : 50

Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD boards such as Apex/AceX/Max/Spartan/Sinfi/TK Base or equivalent and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

PROGRAMMING (using VHDL and Verilog)

1. Write HDL code to realize all the logic gates
2. Write a HDL program for the following combinational designs
 - a. 2 to 4 decoder
 - b. 8 to 3 (encoder without priority & with priority)
 - c. 8 to 1 multiplexer
 - d. 4 bit binary to gray converter
 - e. Multiplexer, de-multiplexer, comparator.
3. Write a HDL code to describe the functions of a Full Adder Using three modeling styles.
4. Write a model for 32 bit ALU using the schematic diagram shown below
A (31:0) B (31:0)
Out
 ALU should use combinational logic to calculate an output based on the four bit op-code input.
 ALU should pass the result to the out bus when enable line in high, and tri-state the out bus when the enable line is low.
 ALU should decode the 4 bit op-code according to the given in example below.

OPCODE ALU OPERATION

1. A + B
2. A – B
3. A Complement
4. A * B
5. A AND B
6. A OR B
7. A NAND B
8. A XOR B

5. Develop the HDL code for the following flip-flops, SR, D, JK, T.

Opcode (3:0)

Enable

6. Design 4 bit binary, BCD counters (Synchronous reset and Asynchronous reset) and “any sequence” counters

INTERFACING (at least four of the following must be covered using VHDL/Verilog)

1. Write HDL code to display messages on the given seven segment display and LCD and accepting Hex key pad input data.
2. Write HDL code to control speed, direction of DC and Stepper motor.
3. Write HDL code to accept 8 channel Analog signal, Temperature sensors and display the data on LCD panel or Seven segment display.
4. Write HDL code to generate different waveforms (Sine, Square, Triangle, Ramp etc.,) using DAC change the frequency and amplitude.
5. Write HDL code to simulate Elevator operations
6. Write HDL code to control external lights using relays.
